

**PATENT****Attorney Docket No.: 10008023-1**  
**U.S. Patent Application Serial No.: 09/982,020****REMARKS**

Favorable reconsideration of this application is respectfully requested in view of the amendments above and the following remarks. Claims 1-27, 29 and 31 are pending, of which claims 1, 18 and 25 are independent.

Claims 1, 2, 4-16, 18-21, 23-28, 30, and 31 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Aizikowitz et al. Claims 3, 17, 22, and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Aizikowitz et al. in view of Luch et al. These rejections are respectfully traversed for at least the reasons set forth below.

**Claim Rejections Under 35 U.S.C. §102**

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereof functioning in substantially the same way to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

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Claims 1, 2, 4-16, 18-21, 23-28, 30, and 31 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Aizikowitz et al.

According to an embodiment described in the Applicants' specification, operands are assigned to real registers by selecting a class and possibly a subclass of registers and identifying a register in the particular class and subclass to store each operand. For example, a table may store bit vectors identifying properties, such as class and subclass (See specification, page 4, lines 20-30), for each real register, and this table may be used for register allocation.

Claim 1 recites, "selecting a class of real registers operable to store said operand;" and "selecting at least one subclass of said selected class of real registers, wherein said at least one subclass includes a register to store said operand." Aizikowitz et al. fails to teach selecting a subclass of a class of real registers operable to store an operand.

The rejection cites column 1, lines 49-67 in Aizikowitz et al. as allegedly teaching the claimed selecting a class of real registers. Lines 35-47 in Aizikowitz et al. disclose symbolic registers can be local or global. The symbolic registers are not real registers. Instead, the symbolic registers refer to the data to be allocated to real, physical, hardware registers. See Aizikowitz et al., column 1, lines 27-32.

Aizikowitz et al. also discloses the symbolic registers are mapped to physical hardware registers, such as by the global and local register allocators described in lines 49-67. Lines 51-54 discuss hardware registers that have global lifetimes. In particular, Aizikowitz et al. discloses a local register allocator may have to perform store and load operations for hardware registers with global lifetimes, which may include registers storing data that overlaps more than one block. Aizikowitz et al., however, fails to teach selecting a particular

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class of real registers and at least one subclass of the class for storing an operand. Instead, Aizikowitz et al. simply describes the type of data being stored in the hardware registers, such as global or local symbolic registers, and does not select a particular class and subclass of hardware registers to store the data. The rejection appears to allege that storing a particular type of data in a hardware register constitutes selecting a class and subclass of real registers to store the data. This is incorrect, because the hardware registers in Aizikowitz et al. may be arbitrarily selected and there is no teaching in Aizikowitz et al. that a particular class or subclass of registers are selected for storing data. For example, Aizikowitz et al. does not disclose a table or some other means for determining a class and subclass of a hardware register, and thus Aizikowitz et al. does not teach or suggest selecting a class and subclass of a hardware register operable to store an operand.

The rejection also cites column 4, lines 40-46 and column 2, lines 15-35 in Aizikowitz et al. as allegedly teaching selecting a subclass of real registers within a particular class. Column 4, lines 40-46 of Aizikowitz et al. discloses that after source code is converted to an intermediate representation 12, portions of the intermediate representation, shown as 10a-d in figure 2, are assigned to hardware registers. Aizikowitz et al. fails to teach assigning portions of intermediate code to hardware registers includes selecting a class and subclass of hardware registers to store the portions of intermediate code. Again, the rejection appears to incorrectly allege that storing a particular type of data, such as a portion of intermediate code, in a hardware register constitutes selecting a class and subclass of real registers to store the data. On the contrary, Aizikowitz et al. fails to teach or suggest anything about the type of hardware register, such as a class and subclass of the register, selected to store the portion of intermediate code.

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Column 2, lines 15-35 of Aizikowitz et al. describes a type of data to be stored in hardware registers. In particular, live ranges of data are identified. Aizikowitz et al. discloses in column 2, lines 35-65 using an interference graph. There may be an insufficient number of hardware registers to assign to the live ranges, and thus a live range may have to be "spilled". Aizikowitz et al. appears to disclose predicting, using the interference graph, that at some point of executing a program there may be an insufficient number of hardware registers to store live ranges and thus a spilling operation may be performed to provide a hardware register for storing data.

The rejection appears to allege that storing live ranges in a hardware register constitutes selecting a class of real registers (the global life time register) and selecting at least one subclass of the class (the live range). Selecting a hardware register containing live data does not necessarily require selecting a hardware register in a particular class and subclass. Instead, any hardware register may be arbitrarily selected, regardless of determining the class or subclass of the register.

Claim 4 recites, "determining whether a register included in said first set of subclasses is available to store said operand; and in response to said register being available, storing said operand in said register." Claim 6 recites, "selecting a second set of subclasses within said selected class in response to said register not being available in said first set of subclasses similar features for a second subset". Claim 8 recites, "selecting a third set of subclasses within said selected class in response to a register in said second set of subclasses not being available". None of these features, including three sets of subclasses, and the features recited in the remaining claims dependent on claim 1 are taught by Aizikowitz et al.

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Claim 18 recites, "allocating a plurality of real registers to store a plurality of operands from said intermediate code while generating the intermediate code."

Column 4, lines 40-46 of Aizikowitz et al. discloses that after source code is converted to an intermediate representation 12, portions of the intermediate representation, shown as 10a-d in figure 2, are assigned to hardware registers. Aizikowitz et al., however, fails to teach allocating a plurality of real registers to store a plurality of operands from said intermediate code while generating the intermediate code. Instead, Aizikowitz et al. discloses that after source code is converted to an intermediate representation 12, portions of the intermediate representation are assigned to hardware registers. Accordingly, claims 19-21 and 23-24 are believed to be allowable.

Claim 25 has been amended to recite features similar to claim 1, and thus claims 25-27 and 31 are also believed to be allowable. The features of claims 28 and 30 have been combined with claim 25 and claims 28 and 30 have been canceled.

**Claim Rejection Under 35 U.S.C. §103**

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

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Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

Claims 3, 17, 22, and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Aizikowitz et al. in view of Lueh et al.

The rejections of claims 3, 17, 22 and 29 combine Lueh et al. with Aizikowitz et al. to teach a caller-saved class. However, neither Lueh et al. nor Aizikowitz et al. teach or suggest selecting a caller-saved class for storing an operand. Thus, these claims are also believed to be allowable.

**PATENT**Attorney Docket No.: 10008023-1  
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In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

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